

HiPerFET™

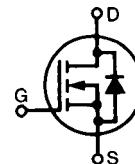
Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr} , HDMOS™ Family

IXFH 76 N06-11
IXFH 76 N06-12
IXFH 76 N07-11
IXFH 76 N07-12

V_{DSS}	I_{D25}	$R_{DS(on)}$
60 V	76 A	11 mΩ
60 V	76 A	12 mΩ
70 V	76 A	11 mΩ
70 V	76 A	12 mΩ

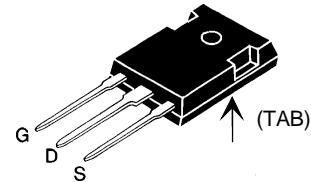
Preliminary data sheet



Symbol	Test Conditions	Maximum Ratings		
V_{DSS}	$T_j = 25^\circ\text{C}$ to 175°C	N06	60	V
		N07	70	V
V_{DGR}	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 10\text{ k}\Omega$	N06	60	V
		N07	70	V
V_{GS}	Continuous		± 20	V
V_{GSM}	Transient		± 30	V
I_{D25}	$T_c = 25^\circ\text{C}$ (Chip capability = 125 A)		76	A
I_{D119}	$T_c = 119^\circ\text{C}$, limited by external leads		76	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}		304	A
I_{AR}	$T_c = 25^\circ\text{C}$		100	A
E_{AR}	$T_c = 25^\circ\text{C}$		30	mJ
E_{AS}			2	J
dv/dt	$I_s \leq I_{DM}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_j \leq 150^\circ\text{C}$, $R_G = 2\Omega$		5	V/ns
P_D	$T_c = 25^\circ\text{C}$		360	W
T_j			-55 ... +175	$^\circ\text{C}$
T_{JM}			175	$^\circ\text{C}$
T_{stg}			-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$
M_d	Mounting torque		1.15/10	Nm/lb.in.
Weight			6	g

Symbol	Test Conditions	Characteristic Values		
		($T_j = 25^\circ\text{C}$, unless otherwise specified)	min.	typ.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	N06	60	V
		N07	70	V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4\text{ mA}$		2.0	3.4 V
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100\text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0\text{ V}$	$T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		100 μA 500 μA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$ Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle $d \leq 2\%$	76N06/N07-11 76N06/N07-12		11 mΩ 12 mΩ

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard package JEDEC TO-247 AD
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

Advantages

- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

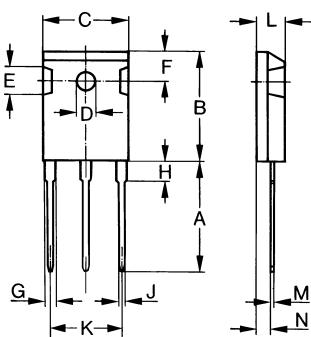
Symbol	Test Conditions	Characteristic Values			
		($T_J = 25^\circ\text{C}$, unless otherwise specified)	min.	typ.	max.
g_{fs}	$V_{DS} = 10\text{ V}$; $I_D = 40\text{ A}$, pulse test	30	40	S	
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$	4400		pF	
		2000		pF	
		1200		pF	
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	$V_{GS} = 10\text{ V}$, $V_{DS} = 50\text{ V}$, $I_D = 30\text{ A}$ $R_G = 1\Omega$ (External)	40		ns	
		70		ns	
		130		ns	
		55		ns	
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 40\text{ A}$	240		nC	
		30		nC	
		120		nC	
R_{thJC}			0.42	K/W	
R_{thCK}			0.25	K/W	

Source-Drain Diode

Characteristic Values

Symbol	Test Conditions	Characteristic Values			
		($T_J = 25^\circ\text{C}$, unless otherwise specified)	min.	typ.	max.
I_s	$V_{GS} = 0\text{ V}$			76	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			304	A
V_{SD}	$I_F = I_s$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle $d \leq 2\%$			1.5	V
t_{rr}	$I_F = 25\text{ A}$, $-\text{di}/\text{dt} = 100\text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$ $V_R = 25\text{ V}$ $T_J = 125^\circ\text{C}$	150		ns	
			250	ns	

TO-247 AD (IXFH) Outline



Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	19.81	20.32	0.780	0.800
B	20.80	21.46	0.819	0.845
C	15.75	16.26	0.610	0.640
D	3.55	3.65	0.140	0.144
E	4.32	5.49	0.170	0.216
F	5.4	6.2	0.212	0.244
G	1.65	2.13	0.065	0.084
H	-	4.5	-	0.177
J	1.0	1.4	0.040	0.055
K	10.8	11.0	0.426	0.433
L	4.7	5.3	0.185	0.209
M	0.4	0.8	0.016	0.031
N	1.5	2.49	0.087	0.102

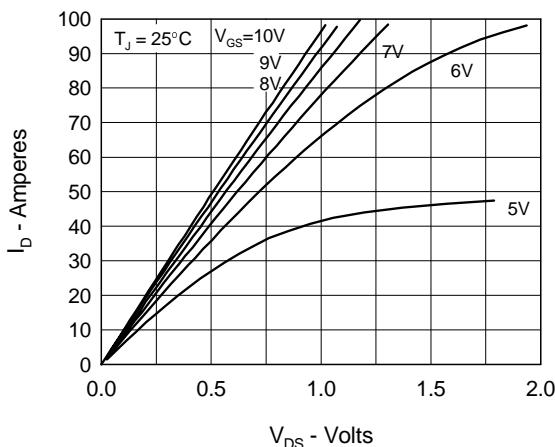
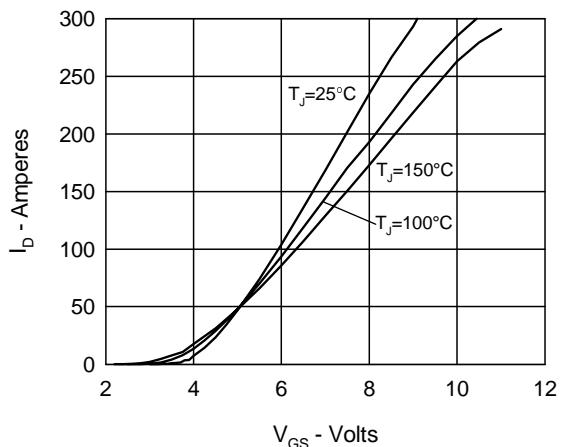
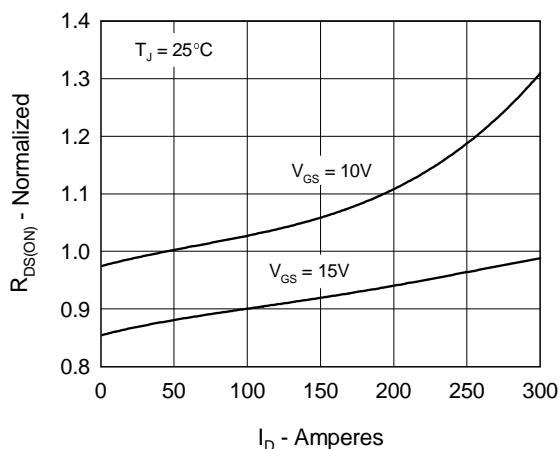
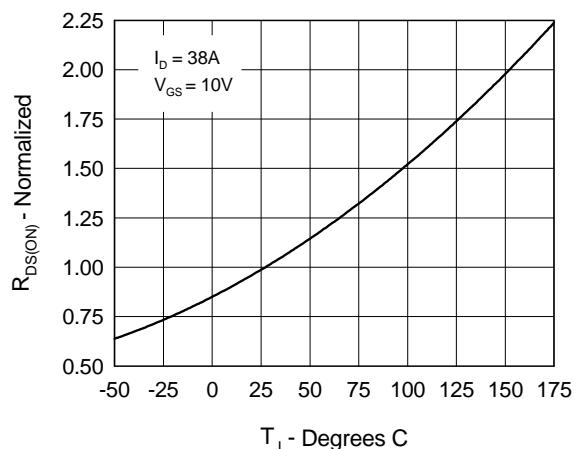
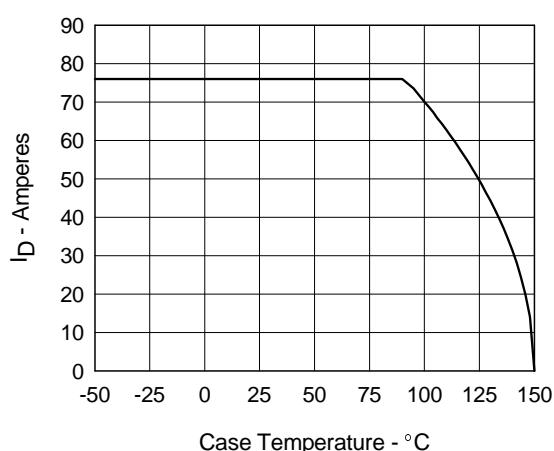
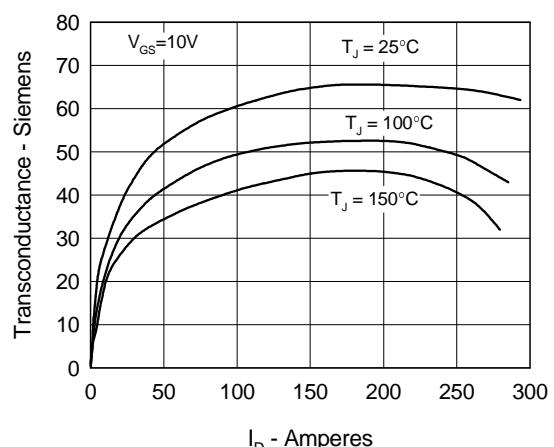
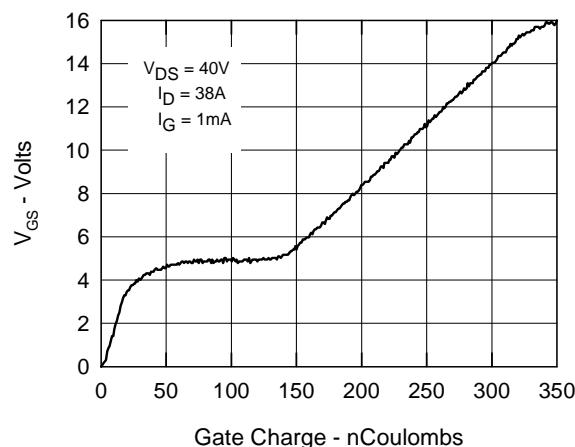
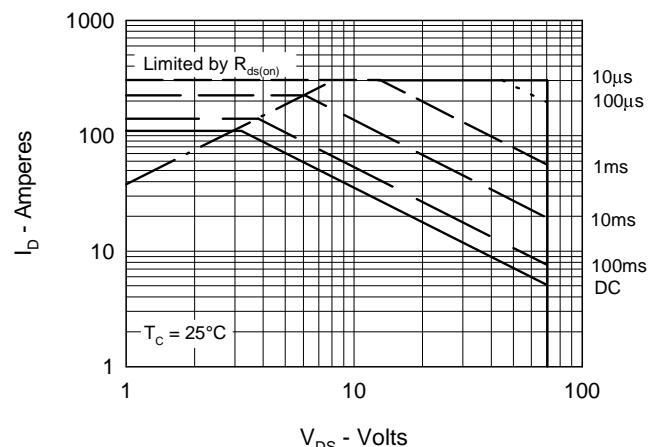
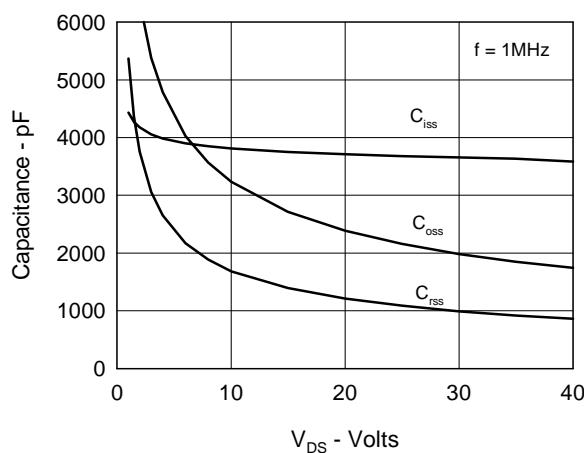
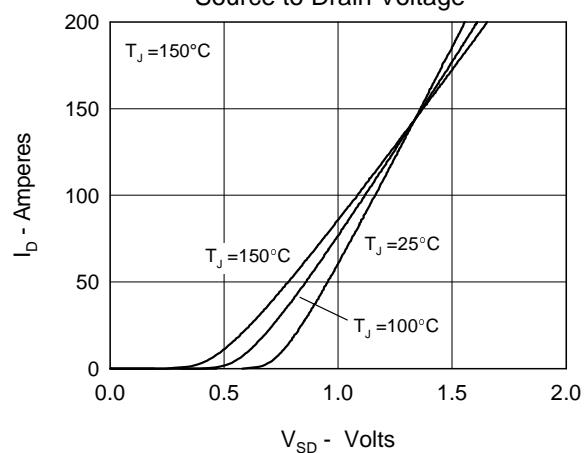
Fig.1 Output Characteristics

Fig. 2 Input Admittance

Fig. 3 $R_{DS(ON)}$ vs. Drain Current

Fig. 4 $R_{DS(ON)}$ Temperature Dependence

Fig. 5 I_D vs. Case Temperature

Fig. 6 Transconductance


Fig. 7 Gate Charge

Fig. 8 Forward Bias Safe Operating Area

Fig. 9 Capacitance Curves

Fig. 10 Source Current vs. Source to Drain Voltage

Fig. 11 Transient Thermal Impedance
